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Addressing the Issues Around Solder Joint Voids in Surface Mount Products

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Types of voids

- Macrovoids
- Planar Microvoids
- Shrinkage Voids
- Micro-Via Voids
- IMC Microvoids
- Pinhole Microvoids

Voids in Solder Joints, Raiyo F, Aspandiar, Intel Corp

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The Genesis

- Interest in voids happened with the introduction of lead free solder and BGA component assembly

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Macrovoids

- Can be found anywhere in the solder joint
- Not unique to any particular solder metallurgy
- Created by the escape of the volatile compounds from the flux and flux chemistries

Voids in Solder Joints, Raiyo F, Aspandiar, Intel Corp

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BGA Process Voids

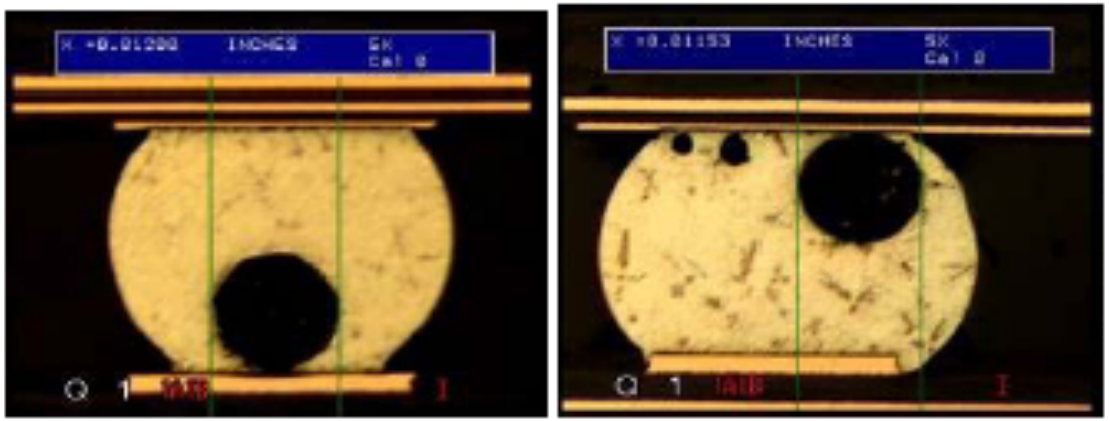

Figure 1. Examples of Process Macrovoids in BGA Solder Joints.

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Voids in Solder Joints, by Raiyo F, Aspandiar, Intel Corp

Concludes:

- "There is general consensus within the industry that Macrovoids do not affect solder joint reliability."

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Planar Microvoids

- Small voids that occur just above the IMC layer at the PCB pad solder interface

Figure 5: A Cross-sectional View of Planar Microvoids in a BGA Solder Joint.

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Planar Microvoids

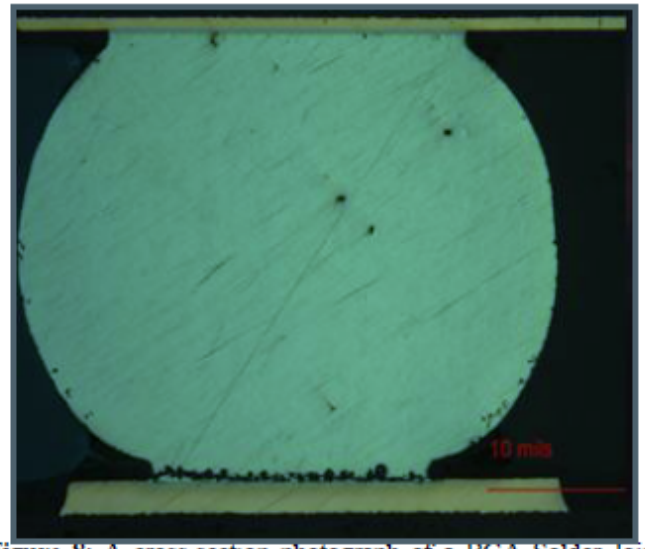

Figure 8: A cross-section photograph of a BGA Solder Joint

Planar Microvoids have been seen to affect solder joint reliability for BGAs, especially if they occur in sufficient density on soldermask defined lands.

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Planar Microvoids

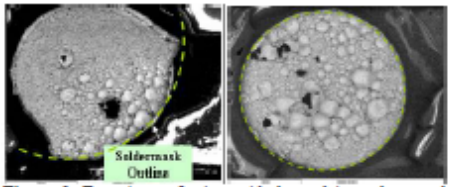

Figure 3. Top views of microvoids located in a plane at the PCB land surface after SMT assembly and solder ball removal. Partially MD-metal-defined (L) and SMD-solder mask defined (R) PCB lands. Microvoids tend to appear more frequently near soldermask edges.

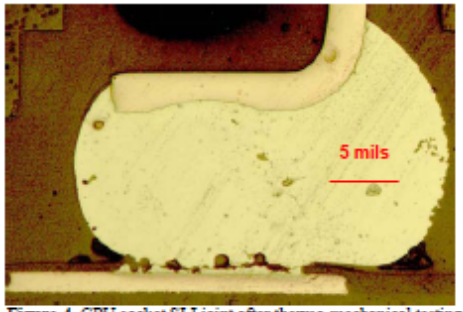

Figure 4. CPU socket SLI joint after thermo-mechanical testing showing a 100% fracture propagating along a plane of microvoids.

Planar Microvoiding In Lead-Free Second-Level Interconnect Solder Joints, by Muffadal Mukadam, Normand Armendariz, Raiyo Aspandiar, Mike Witkowski, Victor Alvarez, Andrew Tong, Betty Phillips and Gary Long

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Planar Microvoids

- According to Coyle, he states: "… conclusion of the investigation is that process voiding can reduce the interconnect fatigue reliability but that void location, not void size or volume fraction, has the greatest influence on fatigue life"

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Put the Macro Void to Rest

- Based upon a research of papers on the voiding subject of BGA Voids,

The location of the void relative to the solder joint failure crack path had a much larger impact than the presence of the void alone

" The Last Will and Testament of the BGA Void, by Dave Hillman, Dave Adams, Tim Pearson, Brad Williams, Britany Petrick, Ross Wilcoxon

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Shrinkage Voids

These are also called sink holes and hot tears

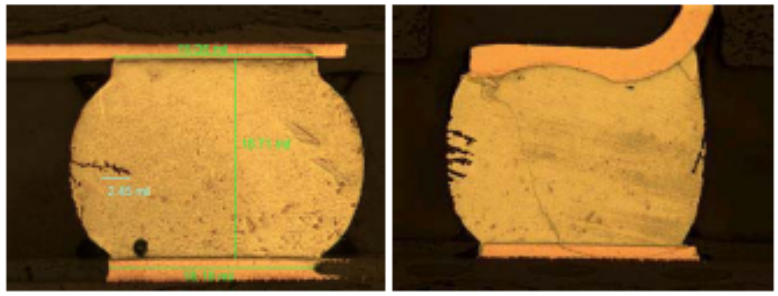

Figure 9. Shrinkage Voids in BGA Solder Joints.

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Micro-Via Voids

Caused by the micro-vias within the pads

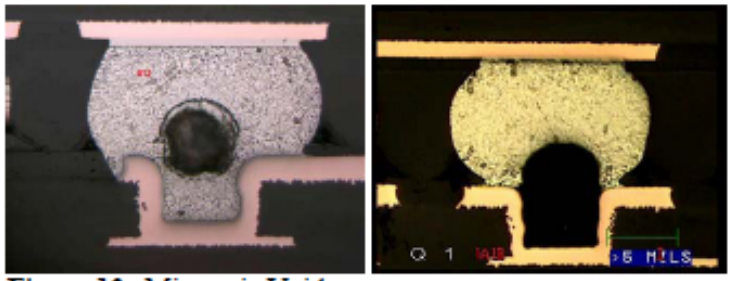

Figure 12. Micro-via Voids.

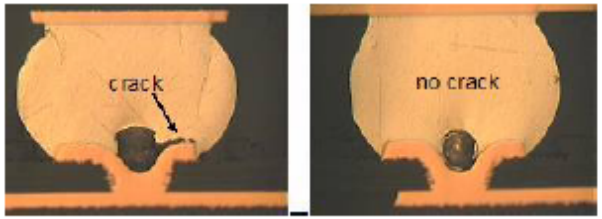

Figure 14. Cracks in a Micro-via Void-containing corner solder joint of a BGA package (Left) and no crack in the adjacent solder joint (Right), which contains a Micro-via Void.

Voids in Solder Joints, Raiyo F, Aspandiar, Intel Corp

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IMC Voids

- Also called Kirkendall Voids

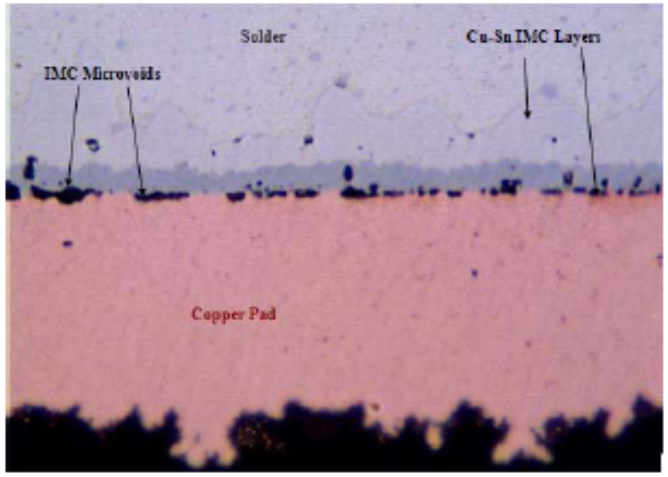

Figure 15: Kirdendall IMC Microvoids at the IMC-Cu Pad interface[30].

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Pinhole Microvoids

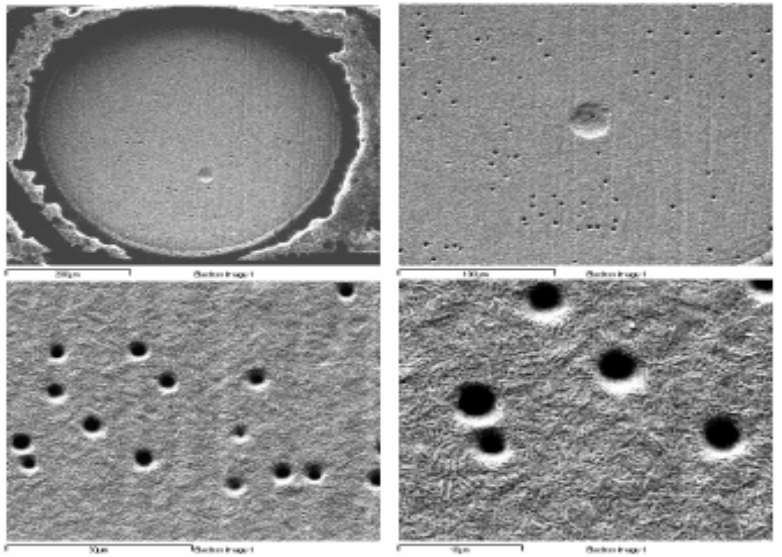

Figure 18: SEM Photographs at different magnifications of the same PCB BGA Land containing pinholes[35].

Voids in Solder Joints, Raiyo F, Aspandiar, Intel Corp

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QFN voids

- Voids beneath the component found by X-ray inspection

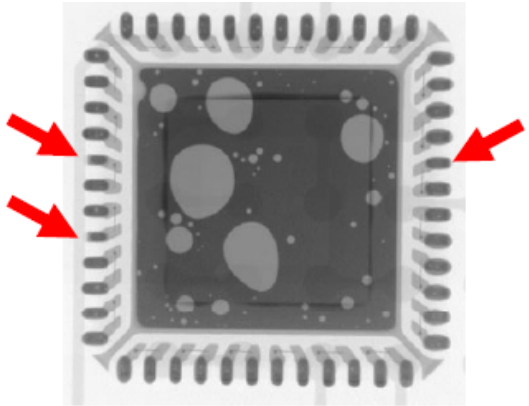

Image 10: X-ray image of a QFN reflowed onto a flexible circuit showing open edge joints (as seen by the shape of, and less material in, the joint – see arrows and compare

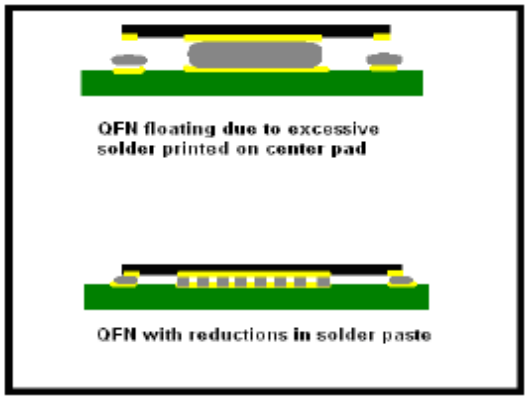

Figure 3.
QFN Floating and
QFN Stabilized with Solder Paste Reduction

COMMON PROCESS DEFECT IDENTIFICATION OF QFN PACKAGES USING OPTICAL AND X-RAY INSPECTION by David Bernard and Bob Willis

OVERCOMING THE CHALLENGES OF THE QFN Package by Karl Seelig and Kevin Pigeon of AIM

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QFN voids

- To reduce the amount of solder different aperture need to be designed
- Use of the window pane helps the distribution of solder

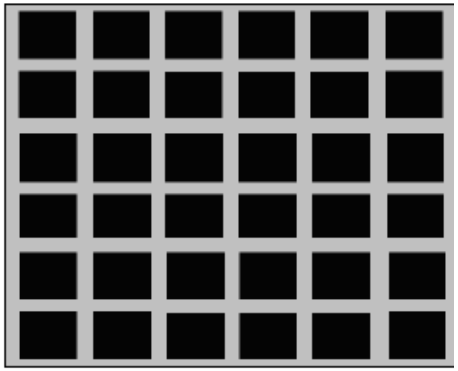

Figure 4.
Window Pane Reduction Design

OVERCOMING THE CHALLENGES OF THE QFN Package by Karl Seelig and Kevin Pigeon of AIM

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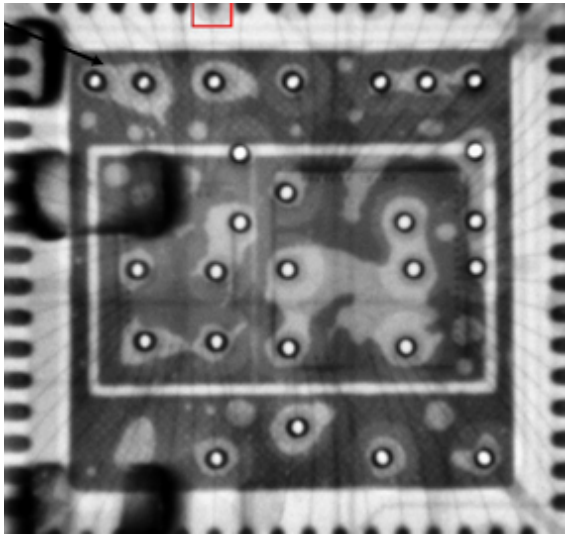
QFN voids

- Vias are the issue in this photo



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QFN voids

- Reduce the aperture in the stencil to allow the escape of the solder paste volatiles.
- Design the product with Vias in pad to reduce the outgassing

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2. *BGA Solder Void Correlation To Via-in-pad, Via Fill, Surface Finish, And Lead-free Solder –A Preliminary Review, Part Three;* by Chrys Shea, Rahul Raut and Lou Picchione
3. *Overcoming The Challenges Of The QFN Package,* by Karl Seelig and Kevin Pigeon
4. *Common Process defect Identification of QFN Packages Using Optical and X-Ray Inspection*, by David Bernard and Bob Willis
5. *Planar Microvoiding In Lead-Free Second-Level Interconnect Solder Joints*, by Muffadal Mukadam, Norman Armendariz, Raiyo Aspandiar, Mike Witkowski, Victor Alvarez, Andrew Tong, Betty Phillips and Gary Long
6. *The Influence of Solder Void Location on BGA Thermal Fatigue Life*, by Richard Coyle, Heather McCormick Peter Read, Richard Popowich and John Osenbach
7. *The Last Will and Testament of the BGA Void,* by Dave Hillman, Dave Adams, Tim Pearson, Brad Williams, Britany Petrick, Ross Wilcoxon

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Thank You

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Further Information

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