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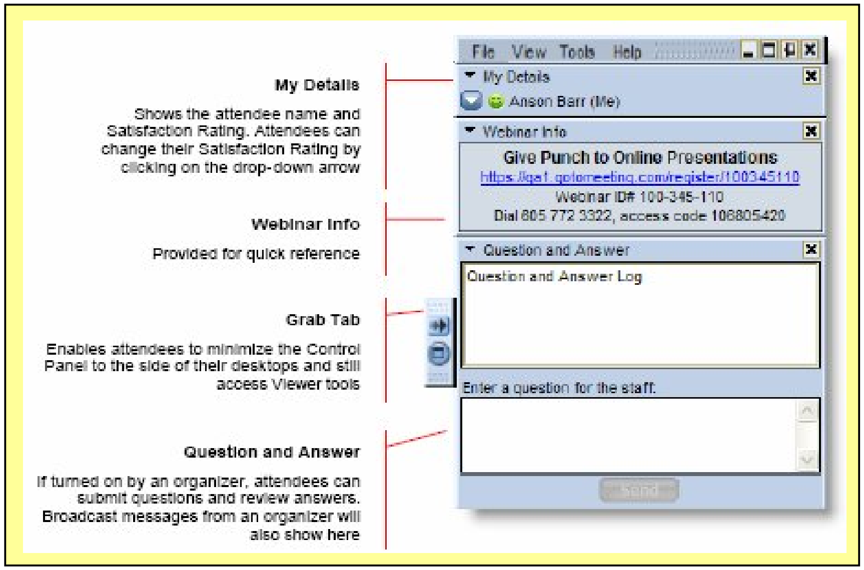

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Board Standards

- IPC-A-600, Acceptability of Printed Boards
- IPC-6012, Qualification and Performance Specification for Rigid Printed Boards
- IPC-2221, Generic Standard on Printed Board Design

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IPC-A-600

- This is the document used to inspect incoming printed circuit boards.
- It has 4 sections:
  - Introduction
  - External observation
  - Internal observation
  - Flexible and flush boards

IPC-A-600 Training

- Two programs exist:
  - CIS – Operator training and is offered in a modular fashion
  - CIT – Trainer certification covers the entire book.

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Series Specifications

IPC-6012 and IPC-2221

- These are the two documents which are invoked in the process of having the printed circuit fabricated.
- These documents provide design information for the artwork, the selection of materials, solder mask selection and functionality, etc.

Series Specifications List

IPC-QL-653	Certification of Facilities that Inspect/Test Printed Wiring Boards, Components and Materials
IPC-CC-830	Qualification and Performance of Electrical Insulating Compound for Printed Board Assemblies
IPC-SM-840	Qualification and Performance of Permanent Solder Mask
IPC-2221	Generic Standard on Printed Board Design
IPC-2251	Design Guide for the Packaging of High Speed Electronic Circuits
IPC-4101	Specification for Base Materials for Rigid and Multilayer Printed Boards
IPC-4103	Specification for Base Materials for High Speed/High Frequency Applications
IPC-4203	Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Wiring and Flexible Bonding Films
IPC-4552	Electroless Nickel/Immersion Gold Plating for Electronic Interconnections
IPC-4553	Specification for Immersion Silver Plating for Printed Circuit Boards
IPC-4562	Metal Foil for Printed Wiring Applications
IPC-4563	Resin Coated Copper Foil for Printed Boards Guideline
IPC-4811	Specification for Embedded Passive Device Resistor Materials for Rigid and Multilayer Printed Boards
IPC-4821	Specification for Embedded Passive Device Capacitor Materials for Rigid and Multilayer Printed Boards

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Test Methods

Although taken from IPC-6012, they are part of the IPC-TM-650 series.

- These documents provide directions to perform or conduct certain activities to verify that the product is, in fact, meeting the specifications.

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Test Methods List

2.1. 1E 05/04 Microsectioning
2.1.1.2A 05/04 Microsectioning, Semi or Automatic Technique Microsection Equipment (Alternate)
2.3. 15D 05/04 Purity, Copper Foil or Plating
2.3.25C 02/01 Detection and Measurement of Ionizable Surface Contaminants
2.3.38C 05/04 Surface Organic Contaminant Detection Test
2.3.39C 05/04 Surface Organic Contaminant Identification Test (Infrared Analytical Method)
2.4. 1E 05/04 Adhesion, Tape Testing
2.4. 15A 03/76 Surface Finish, Metal Foil
2.4.18.1A 05/04 Tensile Strength and Elongation, In-House Plating
2.4.21E 05/04 Land Bond Strength, Unsupported Component Hole
2.4.22C 06/99 Bow and Twist
2.4.28.1D 05/04 Adhesion, Solder Resist (Mask), Tape Test Method

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Design Criteria Examples

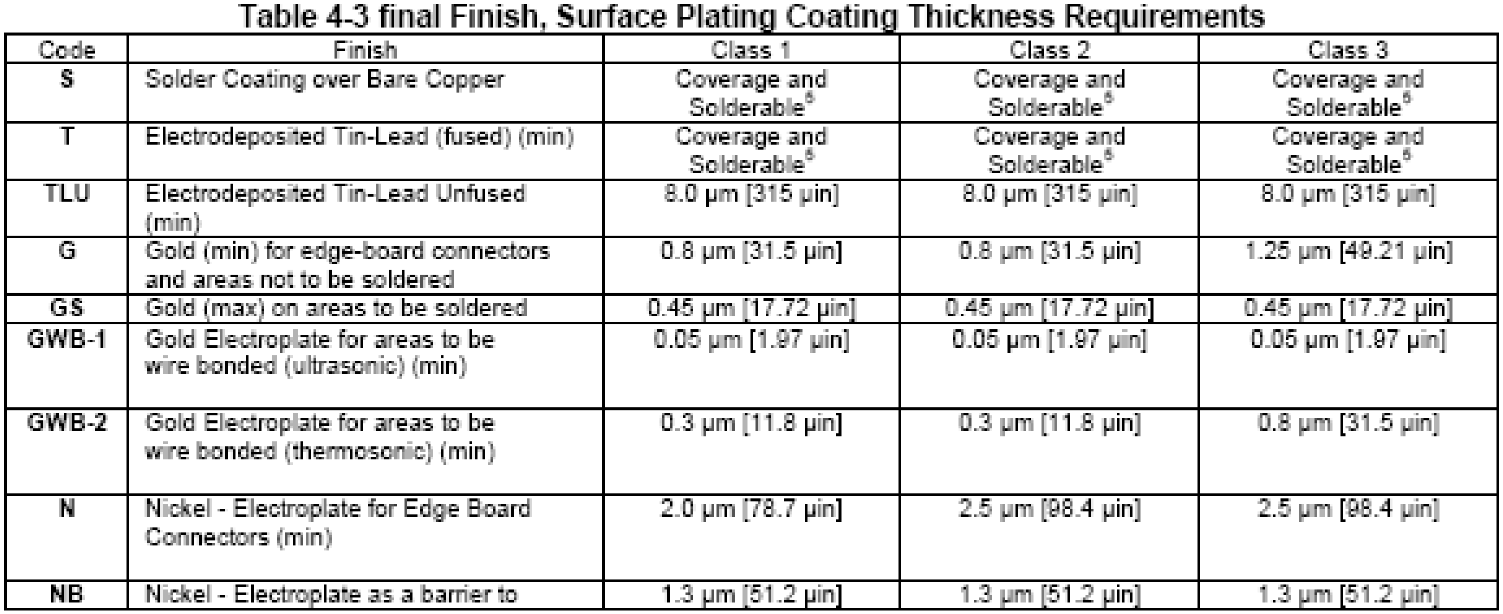

Table 4-3 final Finish, Surface Plating Coating Thickness Requirements

Code	Finish	Class 1	Class 2	Class 3
S	Solder Coating over Bare Copper	Coverage and Solderable[5]	Coverage and Solderable[5]	Coverage and Solderable[5]
T	Electrodeposited Tin-Lead (fused) (min)	Coverage and Solderable[5]	Coverage and Solderable[5]	Coverage and Solderable[5]
TLU	Electrodeposited Tin-Lead Unfused (min)	8.0 µm [315 µin]	8.0 µm [315 µin]	8.0 µm [315 µin]
G	Gold (min) for edge-board connectors and areas not to be soldered	0.8 µm [31.5 µin]	0.8 µm [31.5 µin]	1.25 µm [49.21 µin]
GS	Gold (max) on areas to be soldered	0.45 µm [17.72 µin]	0.45 µm [17.72 µin]	0.45 µm [17.72 µin]
GWB-1	Gold Electroplate for areas to be wire bonded (ultrasonic) (min)	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]
GWB-2	Gold Electroplate for areas to be wire bonded (thermosonic) (min)	0.3 µm [11.8 µin]	0.3 µm [11.8 µin]	0.8 µm [31.5 µin]
N	Nickel - Electroplate for Edge Board Connectors (min)	2.0 µm [78.7 µin]	2.5 µm [98.4 µin]	2.5 µm [98.4 µin]
NB	Nickel - Electroplate as a barrier to	1.3 µm [51.2 µin]	1.3 µm [51.2 µin]	1.3 µm [51.2 µin]

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Design Criteria Examples

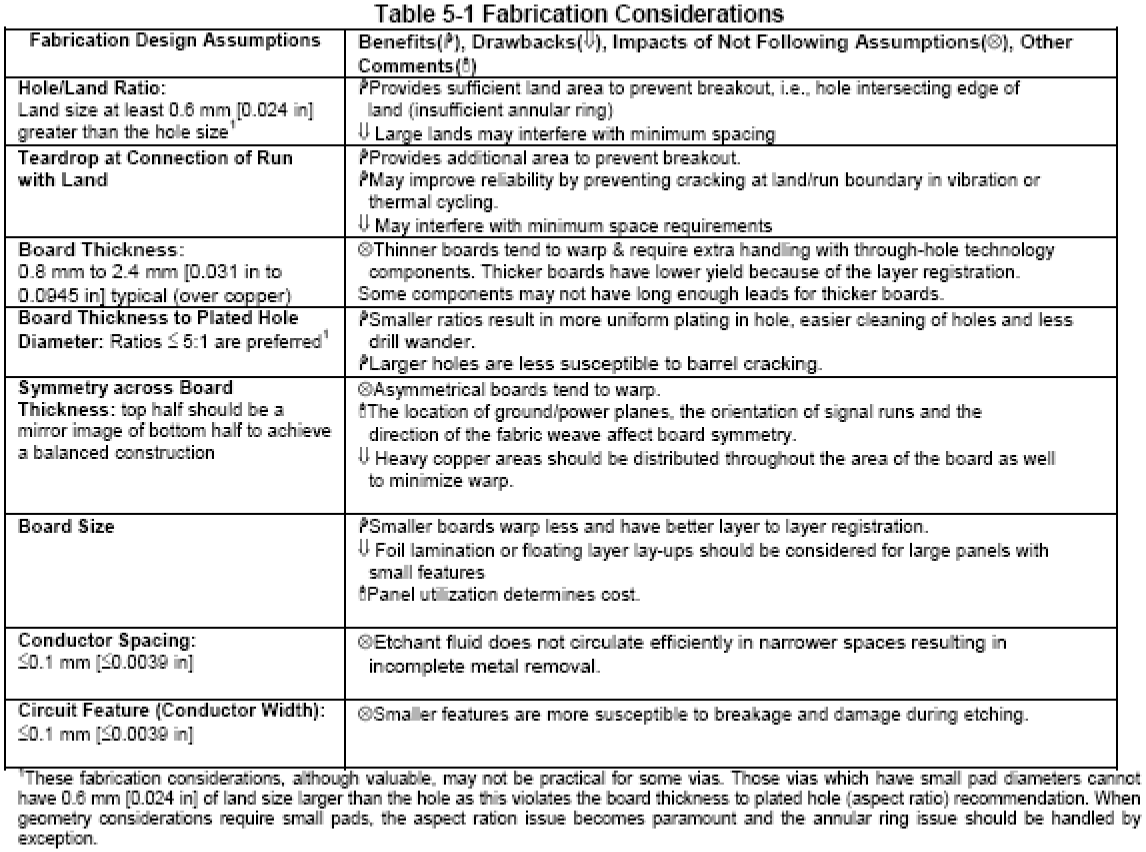

Table 5-1 Fabrication Considerations

Fabrication Design Assumptions	Benefits(⇑), Drawbacks(⇓), Impacts of Not Following Assumptions(⊗), Other Comments(⇕)
Hole/Land Ratio: Land size at least 0.6 mm [0.024 in] greater than the hole size[1]	⇑Provides sufficient land area to prevent breakout, i.e., hole intersecting edge of land (insufficient annular ring) ⇓ Large lands may interfere with minimum spacing
Teardrop at Connection of Run with Land	⇑Provides additional area to prevent breakout. ⇑May improve reliability by preventing cracking at land/run boundary in vibration or thermal cycling. ⇓ May interfere with minimum space requirements
Board Thickness: 0.8 mm to 2.4 mm [0.031 in to 0.0945 in] typical (over copper)	⊗Thinner boards tend to warp & require extra handling with through-hole technology components. Thicker boards have lower yield because of the layer registration. Some components may not have long enough leads for thicker boards.
Board Thickness to Plated Hole Diameter: Ratios ≤ 5:1 are preferred[1]	⇑Smaller ratios result in more uniform plating in hole, easier cleaning of holes and less drill wander. ⇑Larger holes are less susceptible to barrel cracking.
Symmetry across Board Thickness: top half should be a mirror image of bottom half to achieve a balanced construction	⊗Asymmetrical boards tend to warp. ⇕The location of ground/power planes, the orientation of signal runs and the direction of the fabric weave affect board symmetry. ⇓ Heavy copper areas should be distributed throughout the area of the board as well to minimize warp.
Board Size	⇑Smaller boards warp less and have better layer to layer registration. ⇓ Foil lamination or floating layer lay-ups should be considered for large panels with small features ⇕Panel utilization determines cost.
Conductor Spacing: ≤0.1 mm [≤0.0039 in]	⊗Etchant fluid does not circulate efficiently in narrower spaces resulting in incomplete metal removal.
Circuit Feature (Conductor Width): ≤0.1 mm [≤0.0039 in]	⊗Smaller features are more susceptible to breakage and damage during etching.

[1] These fabrication considerations, although valuable, may not be practical for some vias. Those vias which have small pad diameters cannot have 0.6 mm [0.024 in] of land size larger than the hole as this violates the board thickness to plated hole (aspect ratio) recommendation. When geometry considerations require small pads, the aspect ration issue becomes paramount and the annular ring issue should be handled by exception.

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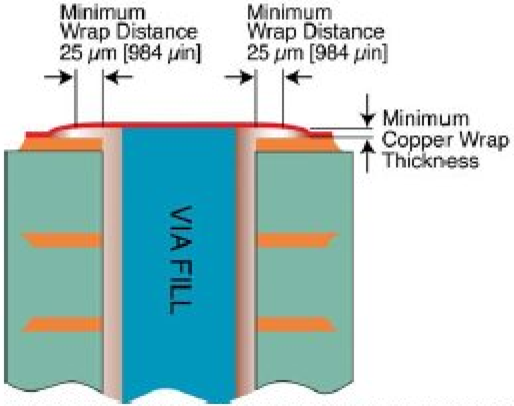
Copper Wrap Plating Thickness



Note: Cap plating, if required, over filled holes is not considered in wrap copper thickness measurements.

Figure 3-13 Surface Copper Wrap Measurement (Applicable to all filled plated-through holes)

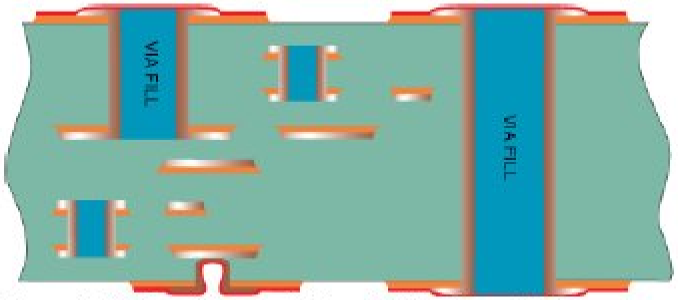


Figure 3-14 Wrap Copper in Type 4 PCB (Acceptable)

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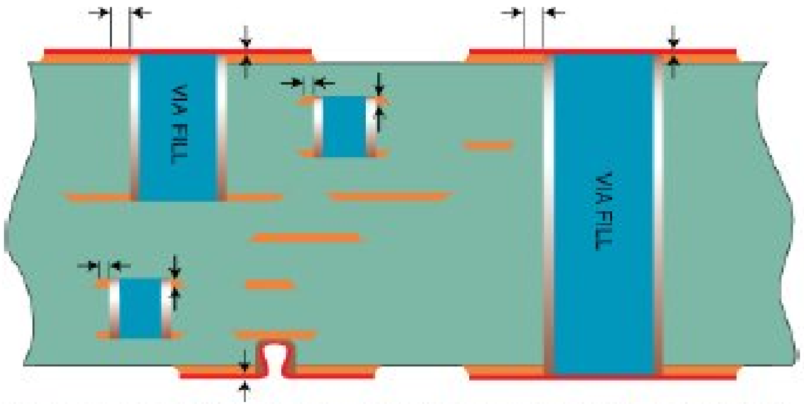
Copper Wrap Plating Thickness



Note: Dimension lines and arrows indicate where wrap copper has been removed.

Figure 3-15 Wrap Copper Removed by Excessive Sanding/Planarization (Not Acceptable)

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IPC-6012 Breakout Criteria

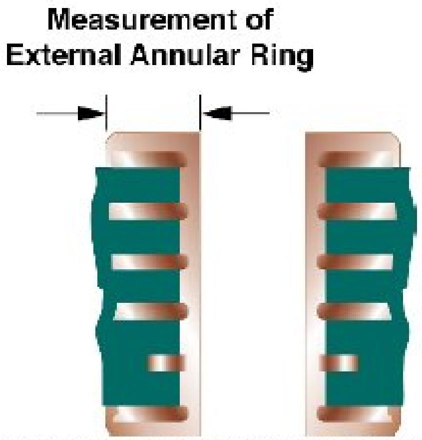
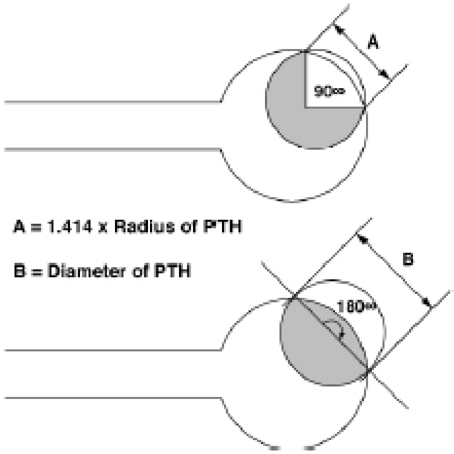


Figure 3-1 Annular Ring Measurement (External)

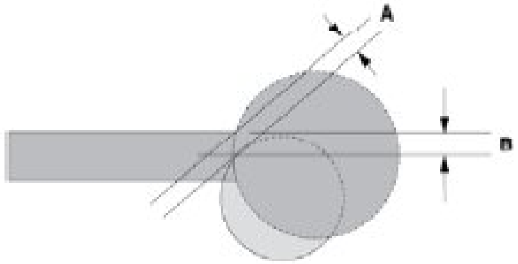


A = 1.414 x Radius of PTH

B = Diameter of PTH

Figure 3-2 Breakout of 90° and 180°

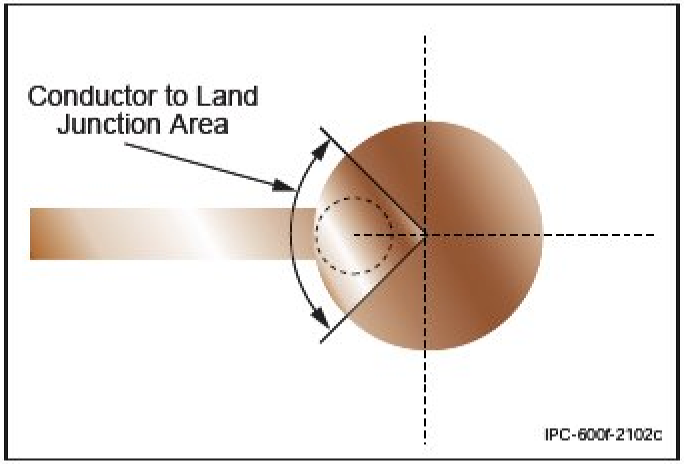
IPC-6012 Conductor Width Criteria



A = Land/Conductor Junction
B = Minimum Conductor Width

Hole breakout shall not reduce the land/conductor junction below the minimum conductor width. This figure depicts a nonconforming condition.

Figure 3-3 Conductor Width Reduction



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IPC-6012 Conductor Thickness Criteria

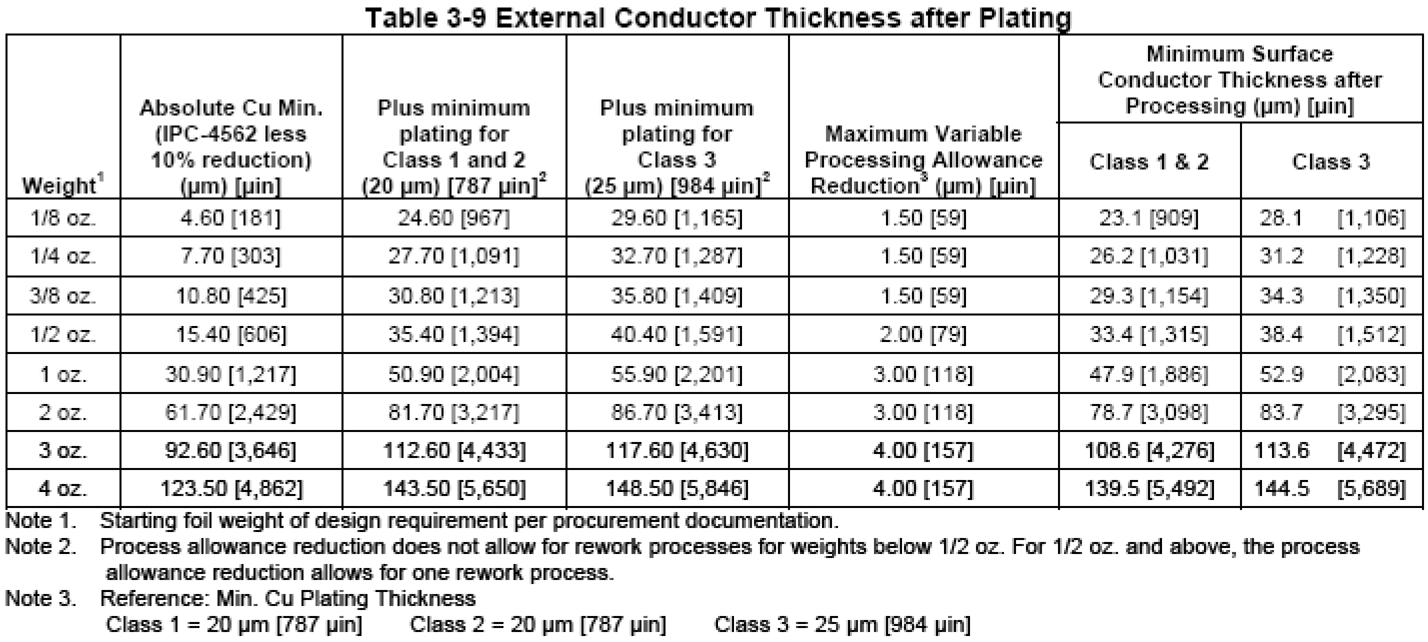

Table 3-9 External Conductor Thickness after Plating

Weight[1]	Absolute Cu Min. (IPC-4562 less 10% reduction) (µm) [µin]	Plus minimum plating for Class 1 and 2 (20 µm) [787 µin][2]	Plus minimum plating for Class 3 (25 µm) [984 µin][2]	Maximum Variable Processing Allowance Reduction[3] (µm) [µin]	Minimum Surface Conductor Thickness after Processing (µm) [µin]	
					Class 1 & 2	Class 3
1/8 oz.	4.60 [181]	24.60 [967]	29.60 [1,165]	1.50 [59]	23.1 [909]	28.1 [1,106]
1/4 oz.	7.70 [303]	27.70 [1,091]	32.70 [1,287]	1.50 [59]	26.2 [1,031]	31.2 [1,228]
3/8 oz.	10.80 [425]	30.80 [1,213]	35.80 [1,409]	1.50 [59]	29.3 [1,154]	34.3 [1,350]
1/2 oz.	15.40 [606]	35.40 [1,394]	40.40 [1,591]	2.00 [79]	33.4 [1,315]	38.4 [1,512]
1 oz.	30.90 [1,217]	50.90 [2,004]	55.90 [2,201]	3.00 [118]	47.9 [1,886]	52.9 [2,083]
2 oz.	61.70 [2,429]	81.70 [3,217]	86.70 [3,413]	3.00 [118]	78.7 [3,098]	83.7 [3,295]
3 oz.	92.60 [3,646]	112.60 [4,433]	117.60 [4,630]	4.00 [157]	108.6 [4,276]	113.6 [4,472]
4 oz.	123.50 [4,862]	143.50 [5,650]	148.50 [5,846]	4.00 [157]	139.5 [5,492]	144.5 [5,689]

Note 1. Starting foil weight of design requirement per procurement documentation.

Note 2. Process allowance reduction does not allow for rework processes for weights below 1/2 oz. For 1/2 oz. and above, the process allowance reduction allows for one rework process.

Note 3. Reference: Min. Cu Plating Thickness
Class 1 = 20 µm [787 µin] Class 2 = 20 µm [787 µin] Class 3 = 25 µm [984 µin]

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Weave Exposure as an Example Topic

What is it? From IPC-6012 it states,

- **3.3.2.5 Weave Exposure**

  Weave exposure or exposed/disrupted fibers are acceptable for all classes provided the imperfection does not reduce the remaining conductor spacing (excluding the area(s) with weave exposure) below the minimum. Refer to IPC-A-600 for more information.

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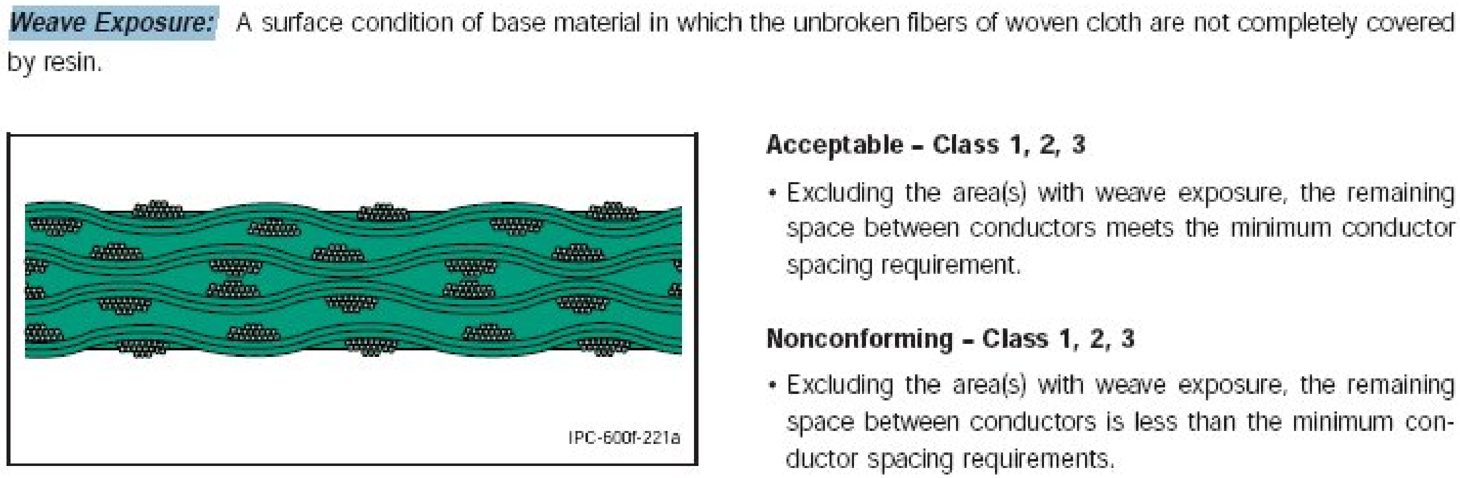
Weave Exposure as an Example Topic

From IPC-A-600



Weave Exposure: A surface condition of base material in which the unbroken fibers of woven cloth are not completely covered by resin.

Acceptable - Class 1, 2, 3

- Excluding the area(s) with weave exposure, the remaining space between conductors meets the minimum conductor spacing requirement.

Nonconforming - Class 1, 2, 3

- Excluding the area(s) with weave exposure, the remaining space between conductors is less than the minimum conductor spacing requirements.

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Weave Exposure as an Example Topic

How does it happen?

- It is a result of the printed circuit lamination process during the foil application where there is excessive pressure and low resin content. When the copper is etched away, it appears on the laminate surface.

Weave Exposure Discussion

- It comes from the raw printed circuit board fabrication process.
- The question I get is:
  - But I see it in assembly and IPC-A-610 states

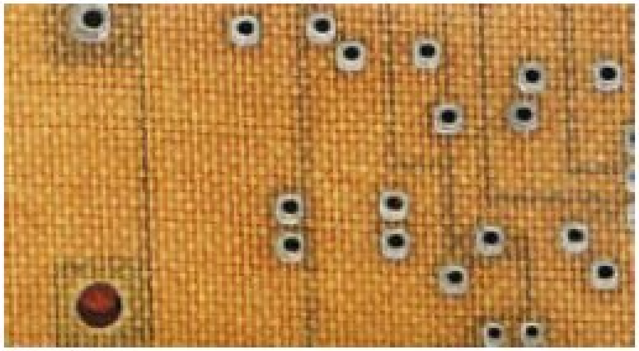


Figure 10-19

Target - Class 1,2,3

- No weave exposure.

Acceptable - Class 1,2,3

- Weave exposure does not reduce the spacing between conductive patterns below specification minimums.

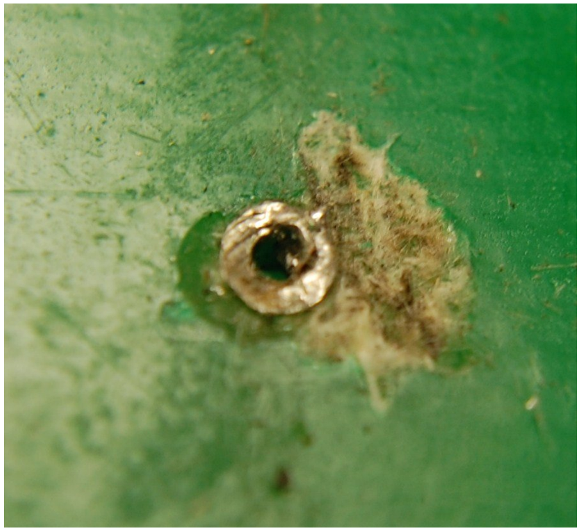
Defect - Class 1,2,3

- Weave exposure reduces the spacing between conductive patterns to less than the minimum electrical clearance.

It Happens During Assembly

- Solder iron destroys the laminate, a tool slips and destroys the laminate. Is this weave exposure?
- If the laminate is cut or scraped and the fibers are broken then, yes, it is weave exposure.

Example of Damage Laminate and Weave Exposure



- Laminate is damaged
  - Exposed fibers
  - Broken fibers
- May violate minimum electrical clearance

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Damaged Laminate

- Weave exposure is considered a conductive surface, so it impacts minimal electrical spacing.
- Can it be fixed? YES
    - Apply an epoxy over the area to seal off the area.

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